



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|--------------------------|---------------------|------------------|
| 10/535,591 | 05/19/2005 | Jan-Willem Van De Waerdt | US020465 | 7635 |

24737 7590 05/07/2007

PHILIPS INTELLECTUAL PROPERTY & STANDARDS

P.O. BOX 3001

BRIARCLIFF MANOR, NY 10510

| |
|----------|
| EXAMINER |
|----------|

CYGIEL, GARY W

| | |
|----------|--------------|
| ART UNIT | PAPER NUMBER |
|----------|--------------|

2188

| | |
|-----------|---------------|
| MAIL DATE | DELIVERY MODE |
|-----------|---------------|

05/07/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/535,591

Applicant(s)

VAN DE WAERDT ET AL.

Examiner

Gary W. Cygiel

Art Unit

2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 May 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 May 2005 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>5/19/2005</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show the titles of the structures in Fig 6a as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The examiner notes that two sets of drawings were submitted on the same day. The set of drawings without any labels and thus subject to similar objections as listed above will not be considered.

Claim Objections

2. Claims 1,10-11,13 and 16 objected to because of the following informalities:

A. Claim 10: The use of --and address field-- is not correct.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 15 is directed towards a method according to Claim 13, but Claim 13 is directed towards an apparatus.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

Art Unit: 2188

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-2,4-9,10-14 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Sherwood et al. **[NPL:Predictor-Directed Stream Buffers]** (hereinafter referred to as Sherwood).

Consider **Claim 1**,

Sherwood teaches a method of data retrieval comprising the steps of:

- providing a first memory circuit (**Fig 3**);
- providing a stride prediction table (SPT) (**Fig 3, Sec 4.2**);
- providing cache memory circuit (**Fig 3**);
- executing instructions for accessing data within the first memory (**Instructions must be executed to access data within the first memory.**);
- detecting a cache miss (**Sec 4.3 ¶3, detects two cache misses in a row**); and
- accessing and updating the SPT only when a cache miss is detected (**Sec 4.3 ¶3m, two-miss allocation filter.**).

Consider **Claims 2 and 16**,

Sherwood teaches a method according to claim 1 wherein the cache memory circuit is a stream buffer (**Fig 3**).

Consider **Claim 4**,

Sherwood teaches a method according to claim 1 wherein the cache memory circuit and the SPT are within a same physical memory space (**Fig 3**).

Consider **Claim 5**,

Sherwood teaches a method according to claim 1 wherein the first memory is an external memory circuit separate from a processor executing the instructions (**Fig 3, data line from/to next lower level of memory.**).

Consider **Claims 6 and 7**,

Sherwood teaches a method according to claim 1 wherein the step of detecting a cache miss includes the steps of:

determining whether an instruction to be executed by the processor is a memory access instruction;

when the instruction is a memory access instruction, determining whether data at a memory location of the memory access instruction is present within the cache; and,

when the data is other than present within the cache, detecting a cache miss, and accessing and updating the SPT only when the cache miss has occurred (**Sec 4.3 ¶3, a cache miss occurs when a requested memory line is not in the cache, therefore requiring the first two limitations of these claims.**).

Consider **Claim 8**,

Sherwood teaches a method according to claim 1, wherein the step of accessing provides a step of filtering that prevents unnecessary access and updates to entries within the SPT **(Sec 4.3)**.

Consider **Claim 10**,

Sherwood teaches a method according to claim 1, wherein the SPT comprises and address field, and where a size of the address field is less than an address space used to index the SPT **(Sec 4.2 ¶5, Table tag size can be reduced by storing only partial address tags.)**.

Consider **Claim 11**,

Sherwood teaches an apparatus comprising:

a stride prediction table (SPT) **(Fig 3,Sec 4.2)**; and

a filter circuit for use with the SPT, the filter circuit for determining instance wherein the SPT is to be accessed and updated, the instances only occurring when a cache miss is detected **(Sec 4.3 ¶3)**.

Consider **Claim 12**,

Sherwood teaches an apparatus according to claim 11 comprising a memory circuit, the memory circuit for storing the SPT therein (**Fig 3**).

Consider **Claim 13**,

Sherwood teaches an apparatus according to claim 12 comprising a cache memory, the cache memory residing within the memory circuit (**Fig 3**).

Consider **Claim 14**,

Sherwood teaches an apparatus according to claim 13, wherein the memory circuit is a single ported memory circuit (**Fig 3, Markov Predictor has single input and single output, Handling a single request at a time.**).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

Art Unit: 2188

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
9. Claims 3,9 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sherwood et al. [**NPL:Predictor-Directed Stream Buffers**] (hereinafter referred to as Sherwood) in view of Handy [**NPL: the Cache Memory book**] (hereinafter referred to as Handy).

Consider **Claim 3,9 and 15**,

Sherwood teaches a method according to claim 1 or 13 respectively, but does not specifically disclose all the details regarding the circuits construction.

Handy does teach these limitations such as:

wherein the cache memory circuit is a random access cache memory
(Handy:Page 28, SRAM cell used in internal cache.)

wherein the cache memory circuit is integral with the processor executing the instructions **(Handy:Page 28, CPU on same chip as on-chip cache.)**

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to implement the circuit construction concepts as taught by Handy in the system of Sherwood because they are notoriously well known concepts in the art. The use of these methods constitutes only design choice and has no novelty in the art.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

A. Breche **[WIPO: International Search Report]** detailed search report for instant application.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary W. Cygiel whose telephone number is (571)270-1170. The examiner can normally be reached on Monday through Thursdays 11:00am-3:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on (571)272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


HYUNG SOUGH
SUPERVISORY PATENT EXAMINER

4-27-07


Gary W. Cygiel
Examiner
Art Unit 2188